Attorney's Docket No. 42P18220

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:	Examiner: Reba I. Elmore
Kevin W. Rudd, et al.	Art Group: 2189
Serial No.: 10/747,977	
Filed: December 29, 2003	
For: **METHOD AND APPARATUS FOR ENABLING VOLATILE SHARED DATA ACROSS CACHES IN A COHERENT MEMORY MULTIPROCESSOR SYSTEM TO REDUCE COHERENCY TRAFFIC**	

APPEAL BRIEF

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir or Madam:

Applicants (hereinafter "Appellants") submit one copy of the following Appeal Brief pursuant to 37 C.F.R. § 41.37 for consideration by the Board of Patent Appeals and Interferences. Appellants also submit herewith a check in the amount of $500.00 to cover the cost of filing the opening brief as required by 37 C.F.R. § 41.20(b)(2). Please charge any additional amount due or credit any overpayment to deposit Account No. 02-2666.

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I. REAL PARTY IN INTEREST

Kevin W. Rudd and Kushagra V. Vaid, inventors of the subject application, assigned their rights to the invention disclosed in the subject application through an Assignment recorded on December 29, 2003, at reel and frame 014860/0751 to Intel Corporation, 2200 Mission College Boulevard, Santa Clara, California 95052. Therefore, Intel Corporation is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this Appeal.

III. STATUS OF CLAIMS

Claims 1-31 are pending in the application. No claims are allowed, no claims are amended and no claims are cancelled. Claims 1-31 stand rejected. Therefore, Appellants appeal the rejection of Claims 1-31.

IV. STATUS OF AMENDMENTS

No amendments were filed subsequent to the final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 recites a method comprising filling a cache line 203 (page 9, paragraph [0026], lines 21-28; Figure 2), receiving a first request for a first segment 211, 213 of the cache line (page 10, paragraph [0028], lines 12-14; Figure 2), indicating at least the first segment 211, 213 is in a non-volatile state and sending at least the first segment 211, 213 (page 10, paragraph [0028], lines 12-14; Figure 2) while maintaining the cache line 203 in one of a modified volatile state and an exclusive volatile state. See Application, page 5, paragraph [0014], lines 23-31; page 7, paragraph [0020], lines 19-29; Figure 2.

Claim 9 recites a memory device comprising a plurality of memory segments 207 (page 5, [0014], lines 23-31; Figure 2) to track a volatile status for a subset 211, 213 of a memory segment (page 5, [0014], lines 23-31; Figure 2) and circuitry to allow access to the plurality of memory segments 211, 213 (page 4, paragraph [0011], lines 7-13; Figures 1 and 2).

Claim 13 recites a method comprising executing a first volatile load request (block 401) (page 11, [0031], lines 3-14; Figure 4), placing requested data in a cache line and placing an indication of a shared volatile state associated with the requested data in the cache line (block 405) (page 11, [0032], lines 15-20; Figure 4). See also, Application page 12, paragraph [0035], lines 23-30; page 14, paragraph [0039], lines 3-12.

Claim 17 recites an apparatus comprising means for storing data 107, 121 and means for tracking 203, 207 one of a shared volatile state, a modified volatile state and an exclusive volatile state for the means for storing data. See Application, page 4, paragraph [0011], lines 8-11; page 5, paragraph [0014], lines 23-31 continuing to page 6, paragraph [0014], lines 1-12; Figures 1 and 2. In some embodiments, means for storing data may be a memory structure such as cache 107 or system memory 121. See Application, page 4, paragraph [0011], lines 8-11; Figures 1 and 2. In some embodiments, means for tracking a state for the means for storing data may include cache line 203 or status field 207. See Application, page 5, paragraph [0014], lines 26-28; page 6, paragraph [0014], lines 1-12; Figure 2.

Claim 21 recites a system comprising a first cache 107 in a first central processing unit 101 (page 4, paragraph [0011], lines 2-13; Figure 1) to store a first cache line 203 in one of a shared volatile state, exclusive volatile state, a modified volatile state (page 6, paragraph [0014], lines 1-12; Figure 2) and a second cache in a second central processing unit 103, 105 in communication via a system interconnect 113 with the first cache to store a second cache line (page 4, paragraph [0011], lines 2-13; Figure 1).

Claim 26 recites a processor comprising a pipeline 109 to process instructions in one of program order and out of program order (page 4, paragraph [0011], lines 2-13),

a set of execution units 111 to execute the instructions (page 4, paragraph [0011], lines 2-13) and a set of caches 107 coupled to the pipeline 109 to store data required by the pipeline 109 in one of a modified volatile, exclusive volatile, and shared volatile state (page 6, paragraph [0014], lines 1-12; Figure 1).

Claim 29 recites a machine readable medium having instruction stored therein which when executed cause a machine to perform a set of operations comprising placing data in a cache line 107, indicating the data in the cache line 107 is in one of a modified volatile, exclusive volatile, and shared volatile state and sharing the data in the cache line. See Application, paragraph [0014], page 6, lines 1-7; page 15, paragraph [0043], lines 23-30; Figure 5.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues involved in this Appeal are as follows:

A. Whether Claims 1-31 fail to comply with the enablement requirement under 35 U.S.C. § 112, first paragraph.

B. Whether Claims 1-31 are indefinite under 35 U.S.C. § 112, second paragraph.

All of the claims do not stand or fall together. The basis for the separate patentability of the claims is set forth below.

VII. ARGUMENT

In the outstanding Final Office Action ("Final Action") the Examiner rejects claims 1-31 as being unpatentable under 35 U.S.C. §112, first paragraph for lack of enablement and under 35 U.S.C. §112, second paragraph as being indefinite.

A. Rejection of Claims 1-8 Under 35 U.S.C. §112, First Paragraph

In the outstanding Final Action and subsequent Advisory Action, the Examiner maintains the rejection of claims 1-8 under 35 U.S.C. §112, first

paragraph, for failing to comply with the enablement requirement. Appellants respectfully traverse the rejection for at least the reasons set forth below.

1. Enablement Standard

Appellants respectfully submit the Examiner has not established that the specification fails to enable claims 1-8 for at least the reason that the Examiner fails to apply the proper analysis for determining enablement. In particular, the focus of the examination inquiry on the issue of enablement is whether the specification teaches "those skilled in the art how to make and use the full scope of the claimed invention without 'undue experimentation'." See MPEP §2164.08 citing *In re Wright*, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993). There are several factors to be considered when determining whether the specification fails to meet this standard. These factors include:

(A) The breadth of the claims;

(B) The nature of the invention;

(C) The state of the prior art;

(D) The level of one of ordinary skill;

(E) The level of predictability in the art;

(F) The amount of direction provided by the inventor;

(G) The existence of working examples; and

(H) The quantity of experimentation needed to make or use the invention based on the content of the disclosure. See MPEP §2164.01(a).

In addition, the Examiner should determine the scope of each claim by analyzing the subject matter of each claim as a whole, not by analyzing claim parts individually. See MPEP §2164.08.

2. Claims 1-8

The Examiner fails to follow the above guidelines in concluding the claims lack enablement. Instead, in the Final Action, the Examiner generally alleges claims 1-31 lack enablement for the following reasons:

> "The terminology 'volatile' and 'non-volatile' has been used extensively in the specification and claims without clearly defining the meaning of these terms within the scope of the present invention. Additionally, these terms are already associated with memory devices within the memory arts and cannot be used to now have a different meaning." See Final Action, pages 2-3, paragraph 7.

Appellants respectfully submit the above statement fails to specifically address whether the specification fails to teach one of ordinary skill in the art how to make and use the claimed invention. It takes a considerable amount of conjecture on the Examiner's part to conclude, based on the mere absence of a definition for the terms "volatile" and "non-volatile" in the specification, that one of ordinary skill in the art could not make and use the claimed invention. In particular, these terms are used consistently throughout the specification and are common terms which would be understood by the skilled artisan in the absence of any sort of definition. Moreover, the above statement does not suggest or even contemplate that "undue experimentation" would be required by one of ordinary skill in the art to make and use the claimed invention much less address the 8 enablement factors listed above.

In addition to the above noted flaws in the Examiner's analysis, the Examiner improperly focuses on whether two terms, "volatile" and "nonvolatile," which are used in the specification and found in some of the claims, are clearly defined. As previously pointed out, the analysis must focus on the scope of each claim as a whole, not parts of the claim. Accordingly, for at least the foregoing reasons, the Examiner has not satisfied her initial burden of showing lack of enablement.

Appellants respectfully submit that if the breadth of the claims and what the specification teaches to one of ordinary skill in the art are properly considered, it can be seen that "undue experimentation" is not required to make and use the invention recited in claim 1.

In particular, independent claim 1 recites the following:

> "1. A method comprising: filling a cache line; receiving a first request for a first segment of the cache line; indicating at least the first segment is in a non-volatile state; and sending at least the first segment while maintaining the cache line in one of a modified volatile state and an exclusive volatile state."

Appellants' specification teaches a system for maintaining the coherency of data within caches. See Application, page 1, paragraph [0001]. Coherency may be maintained by indicating the status of the data within cache lines of the cache. The specification teaches that a cache line may include a status field and each cache line may include one or more segments. See Application, page 5, paragraph [0014]. The status field indicates the cache coherence protocol or status for each cache line and/or corresponding cache line segments. See Application, page 5, paragraph [0014], page 8, paragraph [0023]. For example, the specification teaches that the status field may indicate that a cache line is in a modified volatile, exclusive volatile or shared volatile state. See Application, page 6, paragraph [0014], lines 3-5. The specification then goes on to describe the modified volatile, exclusive volatile and shared volatile states of the cache line as follows:

> "the modified volatile state may indicate that cache line 203 contains data that is modified but which may be shared with caches associated with other processors. It may indicate that one segment of the cache line such as lock field 211 may be non-volatile and require that any modifications to this segment of the cache line requires notification of the change to other processors that may or may not hold the line in their caches. It may indicate that another segment of the cache line such as data field 213 may be volatile. The volatile segment of the cache line may be modified without notification to other processors or devices." See Application, page 7, paragraph [0020].
>
> "the shared volatile state may indicate that the contents of the cache line 203 are shared with another processor or device. The shared volatile state may include status information that identifies that some segment of cache line 203 may be in a volatile state and that some segment of the cache line 203 may be in a non-volatile state." See Application, page 7, paragraph [0021].
>
> "the exclusive volatile state may indicate the content of cache line 203 is shared with another process or device and the associated processor or device has ownership. The shared volatile state may include status information that identifies that some segment of cache line 203 may be in a volatile state and that some segment of the cache line 203 may be in a non-volatile state." See Application, page 7, paragraph [0022].

Still further, the specification provides that the status field may indicate that one segment of a cache line is volatile and another is non-volatile. See Application, page 8, paragraph [0023]. The specification then goes on to describe the volatile and non-volatile status indicated by the status field. See Application, page 8, paragraph [0023],

lines 18-30. In particular, the specification recites that a "volatile segment may be a segment that contains data that may be changed by the owning processor without notification to other processors or devices" and a "non-volatile segment may be a segment that may generate a notification to a sharing processor or device if it is modified by the owning processor or device." See Application, page 8, paragraph [0023], lines 18-22.

The specification further includes descriptions and accompanying drawings illustrating processes for management of the cache lines. In particular, Figure 3 illustrates an embodiment where a request for a volatile copy of a cache line is made. In this aspect, the state of the cache line containing previously modified data is set to a modified volatile state in block 307 of Figure 3. The cache then sends the requested data to the source of the request in block 309 of Figure 3 and acknowledges the volatile status of the line and any segments associated with the request. See Application, page 10, paragraph [0028]; Figure 3. The specification provides that the modified volatile state may include a segment that may be designated as volatile and a segment that may be designated as non-volatile. See Application, page 10, paragraph [0029]. The volatile segment may then be modified by the owning processor any number of times and the cache may not need to take any special action to maintain coherence for the modification of the volatile segments. See Application, page 10, paragraph [0029].

Appellants respectfully submit the foregoing excerpts from Appellants' specification teach the manner and process of making and using the invention in terms which correspond in scope to the invention recited in claim 1 and its dependent claims. Accordingly, in view of Appellants' specification one of ordinary skill in the art would be able to make and use the invention without "undue experimentation." Thus, Appellants' specification enables independent claim 1 and its dependent claims. Since claims 1-8 are enabled by the specification, Appellants respectfully request the rejection of claims 1-8 under 35 U.S.C. §112, first paragraph be overturned.

B. Rejection of Claims 9-12 Under 35 U.S.C. §112, First Paragraph

In the outstanding Final Action and subsequent Advisory Action, the Examiner maintains the rejection of claims 9-12 under 35 U.S.C. §112, first paragraph, as failing

to comply with the enablement requirement. Appellants respectfully traverse the rejection for at least the reasons set forth below.

For at least the reasons previously discussed, the Examiner fails to apply the proper analysis in concluding Appellants' specification fails to enable claims 9-12. Thus, for at least this reason, the Examiner has not established claims 9-12 fail to comply with the enablement requirement.

Appellants respectfully submit if the breadth of the claims and what the specification teaches to one of ordinary skill in the art are properly considered, it can be seen that "undue experimentation" is not required to make and use the invention recited in claim 9.

In particular, independent claim 9 recites the following:

> "9. A memory device comprising: a plurality of memory segments to track a volatile status for a subset of a memory segment; and circuitry to allow access to the plurality of memory segments."

Appellants' specification teaches a system for maintaining the coherency of data within caches as described above. In addition to the features previously discussed, the specification teaches that the contents of a cache line may include a data field which contains information tracked by the cache line corresponding to information stored at a given address in memory or related to that address. See Application, page 5, paragraph [0014]. In addition, the cache may be composed of circuitry to allow a processor to access and store data in memory segments or lines of the cache. See Application, page 4, paragraph [0011].

Appellants believe these additional excerpts from Appellants' specification teach the manner and process of making and using the invention in terms that correspond in scope to the invention recited in the claim 9. Accordingly, in view of Appellants' specification, one of ordinary skill in the art would be able to make and use the invention without "undue experimentation." Thus, Appellants' specification enables independent claim 9 and its dependent claims. Since claims 9-12 are enabled by the

specification, Appellants respectfully request the rejection of claims 9-12 under 35 U.S.C. §112, first paragraph be overturned.

C. Rejection of Claims 13-16 Under 35 U.S.C. §112, First Paragraph

In the outstanding Final Action and subsequent Advisory Action, the Examiner maintains the rejection of claims 13-16 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Appellants respectfully traverse the rejection for at least the reasons set forth below.

For at least the reasons previously discussed, the Examiner fails to apply the proper analysis in concluding Appellants' specification fails to enable claims 13-16. Thus, for at least this reason, the Examiner has not established claims 13-16 fail to comply with the enablement requirement.

Appellants respectfully submit if the breadth of the claims and what the specification teaches to one of ordinary skill in the art are properly considered, it can be seen that "undue experimentation" is not required to make and use the invention recited in claim 13.

In particular, independent claim 13 recites the following:

> "13. A method comprising: executing a first volatile load request; placing requested data in a cache line; and placing an indication of a shared volatile state associated with the requested data in the cache line."

Appellants' specification teaches a system for maintaining the coherency of data within caches as described above. In addition to the features previously discussed, the specification and block 401 of Figure 4 of the application teach that a processor or device associated with a cache may generate a volatile load request. See Application, page 11, paragraph [0031]; Figure 4. The specification teaches that the volatile load request accepts data that may have been modified and that a portion of the requested data may be in a volatile state. See Application, page 11, paragraph [0031]. The specification further provides that if the data is retrieved from another cache or similar storage structure where a portion of the data was indicated to be in a volatile state, it

may be stored in the cache line after retrieval with an indication that it is in the shared volatile state. See application, page 11, paragraph [0032]; Figure 4, block 405.

It is clear from the foregoing excerpts from Appellants' specification that the specification teaches the manner and process of making and using the invention in terms which correspond in scope to the invention recited in claim 13. Accordingly, in view of Appellants' specification one of ordinary skill in the art would be able to make and use the invention without "undue experimentation." Thus, Appellants' specification enables independent claim 13 and its dependent claims. Since claims 13-16 are enabled by the specification, Appellants respectfully request the rejection of claims 13-16 under 35 U.S.C. §112, first paragraph be overturned.

D. Rejection of Claims 17-20 Under 35 U.S.C. §112, First Paragraph

In the outstanding Final Action and subsequent Advisory Action, the Examiner maintains the rejection of claims 17-20 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Appellants respectfully traverse the rejection for at least the reasons set forth below.

For at least the reasons previously discussed, the Examiner fails to apply the proper analysis in concluding Appellants' specification fails to enable claims 17-20. Thus, for at least this reason, the Examiner has not established claims 17-20 fail to comply with the enablement requirement.

Appellants respectfully submit if the breadth of the claims and what the specification teaches to one of ordinary skill in the art are properly considered, it can be seen that "undue experimentation" is not required to make and use the invention recited in claim 17.

In particular, independent claim 17 recites the following:

> "17. An apparatus comprising: means for storing data; and means for tracking one of a shared volatile state, a modified volatile state and an exclusive volatile state for the means for storing data."

Appellants' specification teaches a system for maintaining the coherency of data within caches as described above. In addition to the features previously discussed, the

specification teaches the means for storing data may be a memory structure such as the cache containing multiple cache lines for storing data fetched by a processor or a similar device or a system memory. See Application, page 4, paragraph [0011]. The specification further teaches that the contents of a cache line may include a data field which contains information tracked by the cache line corresponding to information stored at a given address in memory or related to that address. See Application, page 5, paragraph [0014]. As previously discussed, the specification describes the shared volatile state, modified volatile state and exclusive volatile states on page 7, paragraph [0020] to page 8, paragraph [0022] of the application.

Appellants believe these additional excerpts from Appellants' specification teach the manner and process of making and using the invention in terms which correspond in scope to the invention recited in the claim 17. Accordingly, in view of Appellants' specification one of ordinary skill in the art would be able to make and use the invention without "undue experimentation." Thus, Appellants' specification enables independent claim 17 and its dependent claims. Since claims 17-20 are enabled by the specification, Appellants respectfully request the rejection of claims 17-20 under 35 U.S.C. §112, first paragraph be overturned.

E. Rejection of Claims 21-25 Under 35 U.S.C. §112, First Paragraph

In the outstanding Final Action and subsequent Advisory Action, the Examiner maintains the rejection of claims 21-25 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Appellants respectfully traverse the rejection for at least the reasons set forth below.

For at least the reasons previously discussed, the Examiner fails to apply the proper analysis in concluding Appellants' specification fails to enable claims 21-25. Thus, for at least this reason, the Examiner has not established claims 21-25 fail to comply with the enablement requirement.

Appellants respectfully submit if the breadth of the claims and what the specification teaches to one of ordinary skill in the art are properly considered, it can be

seen that "undue experimentation" is not required to make and use the subject matter claimed in claims 21-25.

In particular, independent claim 21 recites the following:

> "21. A system comprising: a first cache in a first central processing unit to store a first cache line in one of a shared volatile state, exclusive volatile state, a modified volatile state; and a second cache in a second central processing unit in communication via a system interconnect with the first cache to store a second cache line."

Appellants' specification teaches a system for maintaining the coherency of data within caches as described above. In addition to the features previously discussed, the specification teaches that in an exemplary system, a first processor, a second processor and a third processor may be provided. See Application, page 4, paragraph [0011]. The processors may each have a cache composed of multiple segments or lines and circuitry to allow the processor to access and store data in the lines. See Application, page 4, paragraph [0011]. The specification provides that the processors may be in communication with one another via an interconnect such as a bus. See Application, page 4, paragraph [0012]. The bus may also enable communication between the subcomponents of the processors such as the caches in each processor. See Application, page 4, paragraph [0012]. The specification describes the modified volatile, exclusive volatile and shared volatile states of the cache line and corresponding segments on page 7, paragraph [0020] to page 8, paragraph [0022] of the application. These features are further illustrated in Figure 1 of the Application.

Appellants believe these additional excerpts from Appellants' specification teach the manner and process of making and using the invention in terms which correspond in scope to the invention recited in the claim 21. Accordingly, in view of Appellants' specification one of ordinary skill in the art would be able to make and use the invention without "undue experimentation." Thus, Appellants' specification enables independent claim 21 and its dependent claims. Since claims 21-25 are enabled by the specification, Appellants respectfully request the rejection of claims 21-25 under 35 U.S.C. §112, first paragraph be overturned.

F. Rejection of Claims 26-28 Under 35 U.S.C. §112, First Paragraph

In the outstanding Final Action and subsequent Advisory Action, the Examiner maintains the rejection of claims 26-28 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Appellants respectfully traverse the rejection for at least the reasons set forth below.

For at least the reasons previously discussed, the Examiner fails to apply the proper analysis in concluding Appellants' specification fails to enable claims 26-28. Thus, for at least this reason, the Examiner has not established claims 26-28 fail to comply with the enablement requirement.

Appellants respectfully submit if the breadth of the claims and what the specification teaches to one of ordinary skill in the art are properly considered, it can be seen that "undue experimentation" is not required to make and use the subject matter claimed in claims 26-28.

In particular, independent claim 26 recites the following:

> "26. A processor comprising: a pipeline to process instructions in one of program order and out of program order; a set of execution units to execute the instructions; and a set of caches coupled to the pipeline to store data required by the pipeline in one of a modified volatile, exclusive volatile, and shared volatile state."

Appellants' specification teaches a system for maintaining the coherency of data within caches as described above. In addition to the features previously discussed, the specification teaches that in an exemplary system, instructions and data fetched from the system memory may be managed by a pipeline to allow the instructions and data to be processed in program order or out of program order by execution units further included in the system. See Application, page 4, paragraph [0011]. This feature is further illustrated in Figure 1 of the Application.

Appellants believe these additional excerpts from Appellants' specification teach the manner and process of making and using the invention in terms which correspond in scope to the invention recited in the claim 26. Accordingly, in view of Appellants'

specification one of ordinary skill in the art would be able to make and use the invention without "undue experimentation." Thus, Appellants' specification enables independent claim 26 and its dependent claims. Since claims 26-28 are enabled by the specification, Appellants respectfully request the rejection of claims 26-28 under 35 U.S.C. §112, first paragraph be overturned.

G. Rejection of Claims 29-31 Under 35 U.S.C. §112, First Paragraph

In the outstanding Final Action and subsequent Advisory Action, the Examiner maintains the rejection of claims 29-31 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Appellants respectfully traverse the rejection for at least the reasons set forth below.

For at least the reasons previously discussed, the Examiner fails to apply the proper analysis in concluding Appellants' specification fails to enable claims 29-31. Thus, for at least this reason, the Examiner has not established claims 29-31 fail to comply with the enablement requirement.

Appellants respectfully submit if the breadth of the claims and what the specification teaches to one of ordinary skill in the art are properly considered, it can be seen that "undue experimentation" is not required to make and use the claimed invention.

In particular, independent claim 29 recites the following:

> "29. A machine readable medium having instruction stored therein which when executed cause a machine to perform a set of operations comprising: placing data in a cache line; indicating the data in the cache line is in one of a modified volatile, exclusive volatile, and shared volatile state; and sharing the data in the cache line."

Appellants' specification teaches a system for maintaining the coherency of data within caches as described above. In addition to the features previously discussed, the specification and specifically Figure 5 of the application teach exemplary transition instructions and requests that may initiate transitions or affect the state of a cache line. See Application, page 15, paragraph [0043].

It is clear from the foregoing excerpts from Appellants' specification that the specification teaches the manner and process of making and using the invention in terms which correspond in scope to the invention recited in the claims. Accordingly, in view of Appellants' specification one of ordinary skill in the art would be able to make and use the invention without "undue experimentation." Thus, Appellants' specification enables independent claim 29 and its dependent claims. Since claims 29-31 are enabled by the specification, Appellants respectfully request the rejection of claims 29-31 under 35 U.S.C. §112, first paragraph be overturned.

H. Rejection of Claims 1-31 Under 35 U.S.C. §112, Second Paragraph

In the outstanding Final Action and subsequent Advisory Action, the Examiner rejects claims 1-31 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Appellants regard as the invention. Appellants respectfully traverse the rejection for at least the following reasons.

The proper test for indefiniteness is whether "those skilled in the art would understand what is claimed when the claim is read in light of the specification." See MPEP §2173.02 citing *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 1 USPQ2d 1081, 1088 (Fed. Cir. 1986). If one skilled in the art is able to ascertain the meaning of the claim language in light of the specification, the requirement of definiteness under 35 U.S.C. §112, second paragraph is satisfied. See MPEP §2173.02.

In rejecting the claims on this basis, the Examiner alleges the claim language uses the terms "volatile" and "non-volatile" in conjunction with cache lines and cache line segments without adequately providing meanings within the specification for this use of the terms. See Final Action, page 3. The Examiner alleges the use of the above language is ambiguous because it is not used consistent with the meaning of these terms in the context of memory devices and the terms are further not expressly redefined in the specification. See Final Action, page 4. The Examiner alleges it is not possible from either the specification or the claims to determine the scope of the claim language or determine the metes and bounds of the claims. See Final Action, page 4. Appellants respectfully disagree with the Examiner's findings.

As pointed out by Appellants in the previous response, the terms "volatile" and "non-volatile," whether used in the computer art or any other art, are simply adjectives used to modify the noun they are used in conjunction with. For example, when the term "volatile" is used in the context of a cache line or segment in the phrase "modified volatile state", as it is in the instant application, it indicates the volatility or changeability of the cache line or segment. See, for example, page 7, paragraph [0020] of the application. Such use of the term "volatile" is entirely consistent with the ordinary meaning of this term.

Nevertheless, the Examiner alleges these terms have long established definitions tied to hardware used for memory and Appellants' use of the terms to identify the state of a cache line or segment is outside of the given practice. In support of her position, the Examiner provides several technical definitions for phrases such as "nonvolatile memory," "nonvolatile RAM," "nonvolatile storage," "volatile memory" and "volatile storage." Certainly when the terms "volatile" and "non-volatile" are used in conjunction with nouns such as "storage" or "memory" these terms identify a characteristic of a memory device.

Appellants respectfully submit, however, the Examiner is analyzing the terms "volatile" and "non-volatile" from a very specific context, namely, to describe the physical properties of a memory device (e.g., SRAM v. DRAM). One of ordinary skill in the art would understand that this is not the context in which the terms are used in the instant application. Instead, as is evidenced from Appellants' claims and specification, Appellants are using these terms in the context of caches and more broadly, data coherence management. In the context of data coherence management, the term "volatile" has a standard meaning. This meaning would be clearly understood by one of ordinary skill in the art upon review of Appellants' specification and claims.

In any event, if the definitions of these terms relied upon by the Examiner are reviewed, it can be seen that even in the context of memory or storage, the terms "volatile" or "non-volatile" are used to indicate the changeability or volatility of data within the memory. For example, in the excerpt from the dictionary *Microsoft Press, Computer Dictionary, Third Edition*, included with the Final Action by the Examiner and

attached herewith for the Board's convenience as Exhibit A, the term "volatile memory" is defined as "[m]emory used by a program that can change independently of the program, such as memory shared by another program or by an interrupt service routine" (emphasis added). Appellants respectfully note, the definitions cited by Appellants in the Response to Office Action dated August 11, 2006, such as the definition for "volatile variable" in the context of programming variables, attached herewith for the Examiner's convenience as Exhibit B, are further consistent with this meaning. For example, the term "volatile variable" is defined as "a variable in computer programming which can be modified by processes other than the program" (emphasis added).

In any case, Appellants respectfully note, the terms "volatile" and "non-volatile" are not used in Appellants' specification and claims in phrases such as those the Examiner provides definitions of in the Final Action. Instead, these terms are used in phrases such as "modified volatile state," "exclusive volatile state" and "shared volatile state" to indicate a state of the corresponding cache line. As previously pointed out in the traversal of the rejections under 35 U.S.C. §112, first paragraph, page 7, paragraph [0020] to page 8 paragraph [0022] of Appellants' specification clearly sets forth the manner in which these phrases are used in the context of claims 1-31. Thus, one of ordinary skill in the art would understand that when a cache line is indicated as being in, for example, a "modified volatile state," the cache line may contain data that is modified but which may be shared with other processors. One skilled in the art would further understand in view of Appellants' specification that when a cache line is indicated as being in a "shared volatile state" the contents of the line are shared with other processors and when the cache line is in an "exclusive volatile state" the contents of the line are shared and the associated processor or device has ownership. One skilled in the art would further understand that depending upon the state of the cache line segments, notification of any changes to these segments must be sent to other processors that may or may not have the line in their caches. One of ordinary skill in the art would understand that by indicating or tracking the above cache line states as described and recited in the claims, the system ensures that sharing processors are

notified of data changes or modifications and thus data associated with an address in caches sharing the data is consistent.

In addition, the phrases "non-volatile segment" and "volatile segment" are used to indicate the volatility of segments of the cache line. For example, "non-volatile segment" is used to indicate that if the segment is modified or changed by the owning processor or device the segment may generate a notification to sharing processors to ensure that the coherency of the non-volatile data held in caches of the processors are maintained and the phrase "volatile segment" is used to indicate that a segment contains data that may be modified or changed by the owning processor without notice to other processors. See, for example, Application, page 7, paragraph [0020]; page 8, paragraphs [0021]-[0023]; page 10, paragraph [0030]. In view of the foregoing, one of ordinary skill in the art would understand the use of the terms in this context as referring to the changeability or volatility of the content of the cache line or segment.

For at least the foregoing reasons, the meaning of the terms "volatile" and "non-volatile" in the context of the cache lines and cache line segments are consistent with the plain meaning of the terms and their use is further clarified in the specification. Thus, there is no ambiguity or confusion as to the scope of the language or the meets and bounds of the claims. Accordingly, claims 1-31 are in compliance with 35 U.S.C. §112, second paragraph. For the foregoing reasons, Appellants respectfully request withdrawal of the rejection of claims 1-31 under 35 U.S.C. §112, second paragraph.

Respectfully submitted,

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Dated: March 26, 2007

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web to the United States Patent and Trademark Office on March 26, 2007.

Si Vuong

VIII. CLAIMS APPENDIX

The claims involved in this Appeal are as follows:

1. (Original) A method comprising:

filling a cache line;

receiving a first request for a first segment of the cache line;

indicating at least the first segment is in a non-volatile state; and

sending at least the first segment while maintaining the cache line in one of a modified volatile state and an exclusive volatile state.

2. (Original) The method of claim 1, further comprising:

modifying at least a portion the first segment of the cache line; and

sending a notification of the modification.

3. (Original) The method of claim 1, further comprising:

modifying a second segment of the cache line without generating a notification of the modification; and

indicating the second segment is in a volatile state.

4. (Original) The method of claim 1, wherein the cache line is a part of a first cache associated with a first processor.

5. (Original) The method of claim 4, further comprising:

sending data from the cache line to a second cache associated with a second processor.

6. (Original) The method of claim 3, further comprising:

receiving a second request for a different third segment of the cache line; and

sending at least the third segment of the cache line while maintaining one of the modified volatile state and exclusive volatile state.

7. (Original) The method of claim 6, further comprising:

updating the cache line to indicate the third segment of the cache line is in a non-volatile state.

8. (Original) The method of claim 6, further comprising:

updating the cache line such that only the third segment of the cache line is in a non-volatile state; and

invalidating the cache line from all other processors holding the cache line or sending an updated copy of the cache line to a processor.

9. (Original) A memory device comprising:

a plurality of memory segments to track a volatile status for a subset of a memory segment; and

circuitry to allow access to the plurality of memory segments.

10. (Original) The device of claim 9, wherein the volatile status is a modified volatile status.

11. (Original) The device of claim 9, wherein the volatile status is a shared volatile status.

12. (Original) The device of claim 9, wherein the volatile status is an exclusive volatile status.

13. (Original) A method comprising:

executing a first volatile load request;

placing requested data in a cache line; and

placing an indication of a shared volatile state associated with the requested data in the cache line.

14. (Original) The method of claim 13, further comprising:

executing a load or a second volatile load request for data held in the cache line in a non-volatile state; and

returning the result of the volatile load request.

15. (Original) The method of claim 13, further comprising:

executing a load or second volatile load request for a volatile portion of the cache line and placing the cache line in an invalid state.

16. (Original) The method of claim 13, further comprising:

executing a load or second volatile load request for a volatile portion of the cache line and receiving an updated copy of the cache line in a shared volatile state with requested data in a non-volatile state.

17. (Original) An apparatus comprising:

means for storing data; and

means for tracking one of a shared volatile state, a modified volatile state and an exclusive volatile state for the means for storing data.

18. (Original) The apparatus of claim 17, further comprising:

means for indicating one of a first portion and a second portion of a segment of the means for storing data contains non-volatile data.

19. (Original) The apparatus of claim 17, further comprising:

means for notifying a second means for storing data that a non-volatile data has been modified.

20. (Original) The apparatus of claim 17, further comprising:

means for indicating multiple segments are in one of a volatile and non-volatile state for a line of the means for storing data.

21. (Original) A system comprising:

a first cache in a first central processing unit to store a first cache line in one of a shared volatile state, exclusive volatile state, a modified volatile state; and

a second cache in a second central processing unit in communication via a system interconnect with the first cache to store a second cache line.

22. (Original) The system of claim 21, further comprising:

a first processor associated with the first cache; and

a second processor associated with the second cache.

23. (Original) The system of claim 21, further comprising:

a system memory that is cached by the first and second caches.

24. (Original) The system of claim 21, wherein the first cache line indicates at least one non-volatile segment.

25. (Original) The system of claim 21, wherein the first cache notifies the second cache of a change in the non-volatile portion of a cache line in one of the modified volatile, the exclusive volatile state, and shared volatile state.

26. (Original) A processor comprising:

a pipeline to process instructions in one of program order and out of program order;

a set of execution units to execute the instructions; and

a set of caches coupled to the pipeline to store data required by the pipeline in one of a modified volatile, exclusive volatile, and shared volatile state.

27. (Original) The processor of claim 26, wherein the cache generates a notification upon modification of non-volatile data.

28. (Original) The processor of claim 26, wherein the cache shares data containing a modified portion.

29. (Original) A machine readable medium having instruction stored therein which when executed cause a machine to perform a set of operations comprising:

placing data in a cache line;

indicating the data in the cache line is in one of a modified volatile, exclusive volatile, and shared volatile state; and

sharing the data in the cache line.

30. (Original) The machine readable medium of claim 29, having instructions stored therein which when executed cause a machine to perform a set of operations further comprising:

generating a notification when a non-volatile data portion is modified.

31. (Original) The machine readable medium of claim 29, having instruction stored therein which when executed cause a machine to perform a set of operations further comprising:

indicating the size and position of a non-volatile portion of a cache line.

IX. EVIDENCE APPENDIX

A. Exhibit A

Appellants respectfully submit herewith an excerpt from *Microsoft Press, Computer Dictionary.* 3rd ed. (1997) including the definition of "volatile memory" as Exhibit A. Appellants respectfully submit, this evidence was submitted along with the Office Action dated October 2, 2006.

B. Exhibit B

Appellants respectfully submit herewith a print out from the online database <http://ww.dictionary.com> evidencing the definition of "volatile variable" as Exhibit B. Appellants respectfully submit, this evidence was submitted along with the Response to Office Action submitted on August 11, 2006 and entered by the Examiner.

EXHIBIT A

Microsoft Press Computer Dictionary

Third Edition

Microsoft Press

PUBLISHED BY
Microsoft Press
A Division of Microsoft Corporation
One Microsoft Way
Redmond, Washington 98052-6399

Library of Congress Cataloging-in-Publication Data
Microsoft Press Computer Dictionary. -- 3rd ed.
p. cm.
ISBN 1-57231-446-X
1. Computers--Dictionaries. 2. Microcomputers--Dictionaries.
I. Microsoft Press.
QA76.15.M54 1997
004'.03--dc21
97-15489
CIP

Printed and bound in the United States of America.

2 3 4 5 6 7 8 9 QMQM 2 1 0 9 8 7

Distributed to the book trade in Canada by Macmillan of Canada, a division of Canada Publishing Corporation.

A CIP catalogue record for this book is available from the British Library.

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voice recognition \voys´ rek-əg-nish`ən\ *n. See* speech recognition.

voice synthesis \voys´ sin´thə-sis\ *n. See* speech synthesis.

volatile memory \vol`ə-təl mem´ər-ē, vol`ə-tīl\ *n.* **1.** Memory, such as RAM, that loses its data when the power is shut off. *Compare* nonvolatile memory. **2.** Memory used by a program that can change independently of the program, such as memory shared by another program or by an interrupt service routine.

volt \vōlt\ *n.* The unit used to measure potential difference or electromotive force. One volt is defined as the potential across which 1 coulomb of charge will do 1 joule of work, or the potential generated by 1 ampere of current flowing through 1 ohm of resistance. *See also* electromotive force.

voltage \vōl´təj\ *n. See* electromotive force.

voltage regulator \vōl´təj re`gyə-lā-tər\ *n.* A circuit or circuit component that maintains a constant output voltage despite variations in input voltage. See the illustration.

Voltage regulator. This voltage regulator is style TO-220, one of several types available.

volts alternating current \vōltz` äl-tər-nā-tēng kur´ənt\ *n.* The measure of the peak-to-peak voltage swing of an electrical signal. *Acronym:* VAC (V`A-C´).

volume \vol´yōōm\ *n.* **1.** A disk or tape that stores computer data. Sometimes large hard disks are divided into several volumes, each of which is treated as a separate disk. **2.** The loudness of an audio signal.

volume label \vol`yōōm lā`bəl\ *n.* A name for a disk or tape. MS-DOS systems, which seldom use disk names except in directory listings, use the term *volume label*. Apple Macintosh systems, which often refer to disks by name, use the term *volume name*.

volume name \vol`yōōm nām`\ *n. See* volume label.

volume reference number \vol`yōōm ref´ər-əns num`bər, ref´rəns\ *n. See* volume serial number.

volume serial number \vol`yōōm sēr´ē-əl num`bər\ *n.* The optional identifying volume number of a disk or tape. MS-DOS systems use the term *volume serial number*. Apple Macintosh systems use the term *volume reference number*. A volume serial number is not the same as a volume label or volume name. *Compare* volume label.

VON \V`O-N´\ *n.* Acronym for **v**oice **o**n the **n**et. A broad category of hardware and software technology for real-time voice and video transmission over the Internet. The term was coined by Jeff Pulver, who formed a group called the VON Coalition, which opposes regulation of VON technology and promotes VON to the public.

von Neumann architecture \von noi´mən är`kə-tek-chur\ *n.* The most common structure for computer systems, attributed to the mathematician John von Neumann. It uses the concept of a program that can be permanently stored in a computer and manipulated or made self-modifying through machine-based instructions. Sequential processing is characteristic of von Neumann architecture. Parallel architectures have evolved to improve on the encumbrances of sequential instructions. *See also* parallel computer.

von Neumann bottleneck \von noi`mən bot´l-nek\ *n.* Competition between data and instructions for CPU time. Mathematician John von Neumann was the first to show that a computer based on architecture linking a single processor with memory will actually spend more time retrieving data from memory than processing it. The bottleneck arises when the processor has to trade off between executing a large number of instructions per second and reading in a large amount of data in the same time. *See also* central processing unit.

VPD \V`P-D´\ *n.* Acronym for **v**irtual **p**rinter **d**evice driver. *See* virtual device driver.

EXHIBIT B

1 entry found for *volatile variable*.

volatile variable

<programming> A variable in a computer program which can be modified by processes other than the program. For example, a variable that stores the value of a timer chip (either because it is located at the address of the hardware device or because it is updated on interrupts) needs to be volatile to be useful.

A static variable, on the other hand, maintains its value until the program changes it or it is no longer needed. In addition, volatile variables can be held in the stack whereas static variables are usually stored in a program's data segment.

(1995-05-17)

X. RELATED PROCEEDINGS APPENDIX

There are no related proceedings submitted herewith.